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Icinergy's global view accelerates design closure

SOCarchitect major enhancements close the physical design gap – from architecture to implementation

Ottawa, ON – May 6, 2002 – Icinergy Software today announced availability of release 3 of its flagship SOCarchitect™ product. SOCarchitect is an integrated physical design, analysis and optimization environment that allows designers to quickly capture the earliest possible physical representation of a complex ASIC or system-on-chip (SoC), and use the model to drive downstream flows. This global view of the design helps uncover fundamental design flaws when they are easiest to fix – well before RTL coding begins.

SOCarchitect release 3 introduces significant new timing analysis capabilities that improve visibility and predictability throughout the synthesis and place-and-route flow. Built-in timing analysis creates an accurate picture of chip-level timing to guide the synthesis process. A compact, high-capacity database allows users to maintain a

consistent model of the design right from concept through to GDSII. The new release also includes a number of user-customizable "wizards" that simplify repetitive design tasks, plus support for rectilinear regions.

"SOCarchitect accelerates design closure because it gives ASIC designers an accurate, global view of their physical designs –from concept right through to implementation", said Scott McLellan, CEO and president of Icinergy. "Release 3 tightens timing integration with downstream synthesis and place-and-route flows. The tool calculates realistic block-level synthesis timing constraints that reflect path delay through global routes. This gets designers really close to where they want to be on their first pass through synthesis. Designers can add detail to their global view as it becomes available, and continually analyze and refine the model to ensure that the design meets its constraints."

SOCarchitect's new hierarchical timing budgeting algorithm extracts path information from the tool's virtual router to accurately predict delay through global routes. Designers can hence predict whether the design will meet timing closure, and can tune the architecture to reduce downstream iteration.

Designers begin with an abstract timing model, and gradually assign clock domains and timing constraints as they refine the design architecture. SOCarchitect's timing audit capability ensures that constraints are consistent and complete. This greatly simplifies the task of creating synthesis constraints. As a final step, designers can back-annotate timing results from an initial synthesis run, and use this information to fine-tune the timing model.

A new high-capacity database extends SOCarchitect's power down to GDSII level. Designers can read detailed physical information back into the tool as designs progress through the synthesis and place-and-route flow. This ensures a consistent top-down picture of the design, and allows fine-tuning of the architectural model as implementation-level detail becomes available. The new database scales linearly with design size, so multi-million gate designs load quickly, and fit comfortably within the memory resources of standard PCs and UNIX systems.

SOCarchitect's enhanced process technology editor helps users select the most suitable silicon processes for their designs. Designers can switch process technology in seconds, and immediately see the impact on area, timing, power and routing congestion. This allows designers to verify that their selected silicon process meets their needs.

The new release also introduces a number of design wizards. These application examples illustrate the ease with which users can build custom features around SOCarchitect's standard Tcl/Tk application procedural interface. Included with the release are wizards that help place I/O pads, and generate customized RAM instances.

"Release 3 of SOCarchitect adds predictability throughout the synthesis and place-and-route flow", said McLellan. "Designers can synthesize design blocks within the context of the overall chip, and back-annotate downstream information to continually refine the design. The tool complements established design flows – SOCarchitect users increase their chance of first-pass design closure, and they also maintain the integrity of their trusted tool flow. And since this is a tool for team-based design, it's priced at a point that makes it a one-per-desktop solution."

About Icinergy

Icinergy Software is a privately-held company founded to provide high-level design automation software for complex IC and system-on-chip (SoC) designs. The company is venture funded by JMGCC Investments, whose chairman, John Cooper, is a principal architect of numerous advanced-technology design automation solutions. Icinergy is headquartered in Ottawa, Canada and may be reached on the web at www.icinergy.com or by phone at (866) 253-4359 (toll-free) or (613) 271-6257.

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